silicon based CVD method and then removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(c) a third step of annealing the oxide films at a substrate temperature of 1100 to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$.

14. (Amended) The method of claim 9, wherein [the first step is a step of forming the] each of said grooves [having] has an aspect ratio [d/11] $d/1_{1x}$ of less than 10, which is defined by a dimensional ratio of a depth d to a width [11] 1_{1x} of [openings] an opening at a top of each of said grooves.

15. (Amended) The method of claim 9, [wherein the first step is a step of forming the] further including arranging said grooves [as] in a cyclic line and space [patterns] pattern having a line-and-space ratio [$1_1/1_2$] $1_{1x}/1_{2x}$, [which is] of less than 1.5, and defined as a ratio of minimum space width [1_1] 1_{1x} corresponding to a width of openings of the grooves measured along an axis extending in an x direction to a minimum line width [12] 1_{2x} corresponding to a width of a region sandwiched by [the groove of] said grooves [less than 1.5,] and also measured along [a specified] said x direction.--.

Please add new Claims 24-29 as follows:

--24. The method of claim 15, wherein each of said grooves has an opening having the width 1_{1x}, and a height 1_{1y} measured along a y direction so as to provide a second line-and-space ratio $1_{1y}/1_{2y}$ which is larger than 1.5, with 1_{2y} being a space between the grooves and measured along the y direction.

25. A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) depositing oxide films in the grooves by an organic silicon based CVD method;

(c) annealing the oxide films at a substrate temperature of 1100 to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1/\mu m^2$; and

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

26. A method of manufacturing a semiconductor substrate having shallow trench isolation, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by an organic silicon based CVD method; and

(c) annealing said oxide films at a substrate temperature of 1100 to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of said oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

27. A method of manufacturing a semiconductor substrate having shallow trench isolation, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) burying oxide films in the grooves by an organic silicon based CVD method; and

(c) annealing the oxide films at a substrate temperature of 1100 to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective ring structures to a total integrated Raman intensity, and the ring structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85% of an overall ring structure and said lower order ring structures are substantially less than 15% of the overall ring structure.

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28. A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films as part of inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by an organic silicon based CVD method;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) annealing the oxide films at a substrate temperature of 1100 to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves

is less than $1/\mu m^2$.

29. A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising the steps of:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films as part of inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by an organic silicon based CVD method;

(d) annealing the oxide films at a substrate temperature of 1100 to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1/\mu m^2$; and

(e) removing upper parts of the oxide films so as to planarize a surface of the resulting structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.--.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 9-11 and 14-29 are pending in this application. Claims 16-23 have been withdrawn from consideration. Claims 12 and 13 have been canceled without prejudice or disclaimer. Claims 9, 14, and 15 have been amended and new Claims 24-29 have been added to highlight the present invention without the introduction of any new matter.